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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,879	01/13/2004	De-Wei Lee	B-5353 621646-3	3435

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,879	LEE ET AL.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Horvath et al (US Patent 6,754,745; hereinafter Horvath).

4. As per claim 1, Horvath discloses a method for synchronizing all clock sources of semiconductor devices, comprising:

generating multiple clock sources in a plurality of semiconductor devices [Fig. 6; col. 6, lines 49-67; col. 8, lines 1-7];

designating one semiconductor device having a clock source with the lowest rate clock signal as a master device [Fig. 6; col. 5, lines 16-26; the reference clock is at a frequency that is the lowest common denominator of the other transmit clocks; col. 7, lines 14-17; col. 8, lines 20-26; in master mode];

designating the lowest rate clock signal of the master device as a reference clock source [Fig. 6; col. 5, lines 16-26; the reference clock is at a frequency that is the lowest common denominator of the other transmit clocks; col. 8, lines 20-26; in master mode];

performing, according to the reference clock source, a phase-aligned check on other clock sources in the master device, such that other clock sources of the master device are synchronized with the reference clock source to generate a zeroing signal [Fig. 6; col. 5, lines 15-26; col. 6, lines 49-67; col. 7, lines 15-31; col. 8, lines 1-7, 20-25];

respectively performing, according to the zeroing signal, a phase-aligned check on a local lowest rate clock source in each slave device, such that all local lowest rate clock sources of the slave devices are synchronized with the lowest rate clock signal of the master device to respectively generate an aligning signal [Fig. 6; col. 5, lines 15-26; col. 6, lines 49-67; col. 7, lines 15-31; col. 8, lines 1-7, 20-25]; and

respectively performing, according to the aligning signal, a phase-aligned check on other clock sources in each slave device, such that other clock sources of each slave device are separately synchronized with the local lowest rate clock signal of the respective slave devices, thereby completing clock synchronization for the plurality of semiconductor devices [Fig. 6; col. 5, lines 15-26; col. 6, lines 49-67; col. 7, lines 15-31; col. 8, lines 1-7, 20-25].

5. As per claim 7, Horvath discloses a system for synchronizing all clock sources of semiconductor devices, comprising:

a first semiconductor device having a phase checker and a multi-clock generator including generation of the lowest rate clock source [Fig. 6; the voice server card being a first semiconductor device; col. 5, lines 16-26; col. 7, lines 14-17; the reference clock is at a frequency that is the lowest common denominator of the other transmit clocks; col. 5, lines 40-43; col. 7, lines 24-31; a phase-lock loop; col. 8, lines 1-7, 20-26];

a plurality of second semiconductor devices [Fig. 6; the voice server, the line card and the combo card being a plurality of second semiconductor devices], each having an external phase checker [Fig. 6; PLL 620], an internal phase checker [Fig. 6; PLL 696] and a multi-clock generator including generation of a clock-aligned source [Fig. 6; OSC 695], wherein the external phase checker performs phase alignment according to the zeroing signal, such that the lowest rate clock source and the clock-aligned source having phase synchronization to thus output an

aligning signal to the internal phase checker for phase alignment, thereby synchronizing multiple clock sources generated by each second semiconductor, and thus completing clock synchronization of all semiconductor devices [Fig. 6; col. 5, lines 15-26; col. 6, lines 49-67; col. 7, lines 15-31; col. 8, lines 1-7, 20-25].

6. As per claims 2 and 8, Horvath discloses that the plurality of semiconductor devices are implemented by Field Programmable Gate Array or Application Specific Integrated Circuit [Fig. 6; Voice Server 601 and 602, Line Card 603 and Combo Card 604].

7. As per claims 3 and 9, Horvath discloses that the clock generators are implemented by delay locked loop or digital clock manager [col. 7, lines 25-31; PLL or other clock multiplying device; col. 8, lines 1-7; variety of different sources].

8. As per claim 4, Horvath discloses triggering a phase checker in the master device to sample the clock sources inside the master device for phase alignment [Fig. 6; col. 5, lines 15-26; col. 6, lines 49-67; col. 7, lines 15-31; col. 8, lines 1-7, 20-25; inherent to the system].

9. As per claim 5, Horvath discloses respectively checking the lowest rate clock source of the master device through an external phase checker [Fig. 6; col. 5, lines 15-26; col. 6, lines 49-67; col. 7, lines 15-31; col. 8, lines 1-7, 20-25; PLL].

10. As per claim 6, Horvath discloses that respectively internal phase checkers in each slave device [Fig. 6; col. 5, lines 15-26; col. 6, lines 49-67; col. 7, lines 15-31; col. 8, lines 1-7, 20-25; PLL].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

sks
July 5, 2006

THOMAS LEE
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